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APPLICATION FOR LETTERS PATENT

for

DYNAMIC INTEGRATED CIRCUIT CLUSTERS, MODULES INCLUDING SAME AND METHODS OF FABRICATING

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TITLE OF THE INVENTION

DYNAMIC INTEGRATED CIRCUIT CLUSTERS, MODULES INCLUDING SAME AND METHODS OF FABRICATING

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: The present invention relates to a semiconductor device and, more particularly, to a semiconductor device formed from adjacent dice on a semiconductor wafer.

[0002] State of the Art: Electrical components and circuits have been manufactured for some time in the form of integrated circuits fabricated on wafers of semiconductor materials. Formation of integrated circuits on a semiconductor wafer utilizes various techniques such as etching, doping, and layering for forming active circuits and interconnects. Individual integrated circuits on a wafer are referred to as dice and provide an interface for coupling with external electrical connections. Generally, a die on a wafer is separated from other dice by cutting the wafer along scribe or segmentation lanes thereby forming individual integrated circuit "chips" that may be subsequently packaged for use. Because of the increased integration and miniaturization of electronic systems, a need has arisen for identifying higher density approaches for packaging integrated circuits.

[0003] One approach for improving packaging density of integrated circuits has been to place chips on a circuit board in a vertically stacked arrangement. In such approaches, chips are generally packaged and then the individual packages are stacked in a vertical arrangement. Vertical packages approaches have utilized an intricate and sophisticated cross-wiring approach which modifies the individual chips so that they may be stacked by adding a pattern of metallization, often called rerouting leads, to the surface of the wafer. Such rerouting leads extend from the bond pads of the chip to newly formed bond pads that may be arranged along the terminating edge of the chip. In such a configuration, each modified chip is then cut from the wafer and assembled into a stack such that all of the leads of the modified chips are aligned along the same side of the stack resulting in a vertical interconnection of the individual chips. Such approaches result in only modest volumetric improvements at a great interconnection expense that presents many opportunities for failure as well as requiring intricate assembly approaches.

[0004] Other approaches for arraying or otherwise assembling multiple integrated circuits in a more volume-efficient approach include the formation of memory modules which are formed from individual dice that are assembled individually on a common printed circuit board with each of the pads from an individual die routed to the external printed circuit board which provides the interconnection to an adjacent die or dice. While such an approach reduces the number of packages per die, as a plurality of dice are placed on a single printed circuit board and then packaged into a larger memory module assembly, such an approach still results in significant spacing between each of the individual die in order to accommodate manufacturing processes for externally coupling die pads from one integrated circuit to adjacent integrated circuits. Therefore, there is a need for providing an improved and volumetrically more efficient coupling of integrated circuit chips without incurring significant expense of assembling and interconnecting multiple die for use in a higher assembly package.

BRIEF SUMMARY OF THE INVENTION

[0005] A semiconductor wafer having a plurality of dice thereon is manufactured using conventional processing techniques. The wafer is subjected to probe testing or other testing to identify functional and nonfunctional dice. The locations of the functional dice are analyzed to determine the presence of clusters of functional dice or at least the location of adjacent functional dice. A group of functional dice is identified and an interconnection circuit is formed for routing together the signals of adjacent die at the wafer-level to minimize external interconnections once the dice are segmented into devices. The functional die group, once interconnected, is then segmented from the wafer while maintaining the unitary structural integrity of the functional die group as well as the associated interconnections between dice. Wafer-level interconnection of functional dice reduces volumetric requirements on the next higher assembly as well as reduces interconnection labor and dimensions by maintaining die-to-die interconnection at the semiconductor wafer-level.

[0006] The present invention includes several approaches for forming the interconnection circuit including the identification of functional dice and the formation of the circuit specifically between the functional dice as well as an approach to form an interconnection circuit over entire portions of the semiconductor wafer with the nongrouped portions becoming electrically isolated when individual groups of dice become segmented. The interconnection circuit, in one

embodiment, is formed using redistribution layer techniques for forming electrical contacts with bond pads of individual dice. The interconnection circuit includes conductive segments that are routed between respective bond pads of adjacent or nearly adjacent dice. Another embodiment of the present invention teaches coupling functional dice together that are separated from each other by one or more nonfunctional dice. In such an embodiment, the interconnection circuit may also couple to the bond pad of a nonfunctional die which provides the bridging of electrical conductive segments between functional dice. Techniques are also disclosed for isolating the circuitry of the nonfunctional die to prevent undesirable capacitance or loading of the desired signal. A memory module as well as an electronic system interconnected functional die groups is also encompassed by the present invention.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0007] In the drawings, which illustrate what is currently considered to be the best mode for carrying out the invention;

[0008] FIG. 1 is a plan view of a processed semiconductor wafer comprising a plurality of dice with functional die groups illustrated thereon, in accordance with the present invention;

[0009] FIG. 2 is a detailed illustration of a semiconductor wafer having identified groups of functional die thereon, in accordance with an embodiment of the present invention;

[0010] FIG. 2A is a detailed view of one of the functional die groups and associated interconnection circuit, in accordance with an embodiment of the present invention;

[0011] FIG. 2B is a cross-sectional view of an adjacent die interconnection circuit, in accordance with an embodiment of the present invention;

[0012] FIG. 3 is a detailed view of a semiconductor wafer having groupings of functional die identified thereon;

[0013] FIG. 3A is a detailed view of an adjacent die interconnection circuit for coupling adjacent functional die within a group, in accordance with another embodiment of the present invention;

[0014] FIG. 4 is a view of a memory module for coupling thereon an integral plurality of functional die interconnected according to an embodiment of the present invention;

[0015] FIG. 4A is a cross-sectional view of a functional die group mounted to a substrate of a memory module, in accordance with an embodiment of the present invention;

[0016] FIG. 4B is a cross-sectional view of a functional die group associated with a substrate of a memory module, in accordance with another embodiment of the present invention;

[0017] FIG. 5 is a view of a semiconductor wafer having identified groupings of functional die for interconnecting in accordance with an embodiment of the present invention;

[0018] FIG. 5A is a detailed view of an adjacent die interconnection circuit for coupling nearly adjacent groups of functional die, in accordance with an embodiment of the present invention;

[0019] FIG. 6 is a detailed view of an adjacent die interconnection circuit spanning a nonfunctional die, in accordance with an embodiment of the present invention;

[0020] FIG. 7 is a detailed view of an adjacent die interconnection circuit spanning a nonfunctional die, in accordance with an embodiment of the present invention; and

[0021] FIG. 8 is a diagrammatical view of an electronic system including a memory module configured in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0022] The term "semiconductor wafer" as used herein means and includes a bulk substrate comprised of any of various semiconductive materials including, but not limited to, silicon, silicon-on-saphire (SOS), silicon-on-insulator (SOI), silicon-on-glass (SOG), galium arsenide, iridium phosphide, etc.

[0023] When integrated circuits are formed on a semiconductor wafer, a matrix of functional and nonfunctional dice are produced. Accordingly, a random physical distribution of functional and nonfunctional circuits may be produced as shown for wafer 10 in FIG. 1. Note that some die locations surrounding groups of functional dice have been omitted for clarity. An embodiment of the present invention provides a system for coupling multiple dice at the wafer level and maintaining such wafer-level coupling at the packaged device level to produce dynamic memory clusters of varying multiple-die configurations. FIG. 1 displays functional and nonfunctional dice in a matrix. The matrix size discussed herein is for purposes of example only and should not be construed as limiting the invention to any particular matrix size. The present

invention may be provided using any number of matrix sizes and may be a uniformly similar functional type of integrated circuit or may be a mixture of different functional types of integrated circuits.

[0024] FIG. 1 illustrates test results of the probing or probe testing of wafer 10 wherein functional and nonfunctional dice are identified. Those of ordinary skill in the art appreciate the processes associated with probing a wafer to identify functional and nonfunctional components. In some probing applications, individual dice are singularly probed while in other probing applications a plurality of dice may be simultaneously probed in order to determine their operational capabilities. While each individual die is probed, a mapping of functional dice is maintained in order to minimize and preferably eliminate any subsequent manufacturing or testing processes on nonfunctional die.

[0025] While traditional probe tests record the location and functionality of each die, the present invention also evaluates the functionality of adjacent dice and is concerned with the grouping of dice or possible grouping of dice for the potential creation of memory clusters or groups of adjacent or proximately adjacent functional dice. Several groupings of adjacently located functional dice are illustrated in FIG. 1 with grouping of two functional dice illustrated generally as functional die groups 12. While the abundance of functional die groupings is largely a function of processing yield, it should be appreciated that the clustering or grouping may vary among product and processing variations and the configurations presented are merely illustrative.

[0026] Similarly, groupings of four functional dice are exemplarily illustrated as functional die group 14 with a grouping of eight functional dice illustrated generally as functional die group 16. While horizontally adjacently grouped functional dice are illustrated, the present invention further contemplates other adjacently oriented groupings, including irregularly configured groupings of functional dice, are also within the scope of the present invention.

[0027] FIG. 2 illustrates a detailed view of semiconductor devices, namely interconnected functional die groups 13 and 15, the individual dice of each of which are operably coupled with an adjacent die interconnection circuit in accordance with an embodiment of the present invention. FIG. 2A illustrates a detail of interconnected functional die group 15 comprised of functional dice 18-24 which are illustrated as being arranged in a horizontally adjacent configuration. From previous probe testing, functional dice 18-24 were identified as being operational and further

identified as being adjacently interconnectable, in accordance with an embodiment of the present invention. FIG. 2A illustrates an exemplary pinout configuration for each of functional dice 18-24 illustrated as being linearly configured arrays of bond pads 26-32. By way of example, and not limitation, arrays of bond pads 26-32 are illustrated as being comprised of a plurality of bond pads, for clarity's sake being illustrated as each only including four bond pads. Those of ordinary skill in the art appreciate that integrated circuits generally comprise an appreciable number of bond pads, and in the case of memory devices, include bond pads corresponding to address signals as well as other control signals including power, ground, and reference signals for individually accessing data storage elements. Interconnected functional die group 15 is further comprised of adjacent die interconnection segments 34-38 which are respectively formed between selected bond pads of arrays 26-32 to form a parallel interconnection scheme. Adjacent die interconnection segments 34-38 are preferably formed as patterned conductors through the use of a subsequent wafer level processing technique.

[0028] The adjacent die interconnection segments may be formed as part of a wafer post processing step such as through the use of a redistribution layer process wherein conductive traces formed by deposition and patterning are formed in contact with bond pads and routed away from the bond pads. FIG. 2B illustrates one such process wherein functional dice 18, 20 include bond pads 40, 41 respectively in electrical communication with a contact used for connection to an external device such as conductive bumps 42, 43, each of which may comprise a solder bump or conductive or conductive-filled epoxy bump configured as a ball, column, pillar, or stud. In addition, functional dice 18, 20 include internal conductors 44, 45 in electrical communication with bond pads 40, 41, and the various integrated circuits (not shown) formed on the active surface of functional dice 18, 20. Functional dice 18, 20 also include a passivation layer 46 formed on functional dice 18, 20 with openings 48, 49 through the passivation layer 46 exposing the bond pads 40, 41.

[0029] Adjacent die interconnection circuit 50 is formed on a surface 52 of the passivation layer 46 and may be used to interconnect any external connection such as conductive bumps 42, 43 with the bond pads 40, 41. The adjacent die interconnection circuit 50 includes conductor segment 54 in electrical communication with bond pad 40 and extending away therefrom to bond pad 41 of functional die 20, and an outer passivation layer 56 which covers the conductor

segment 54. The outer passivation layer 56 of the adjacent die interconnection circuit 50 insulates the conductor segment 54, and apertures may be formed therethrough to locate and facilitate the formation of conductive bump 42, 43. Both passivation layer 46 and outer passivation layer 56 may comprise a dielectric material, with suitable materials for outer passivation layer 56 including polymers such as polyimide, glasses such as PSG, BSG or BPSG, or oxides, such as SiO_2.

[0030] The present invention contemplates the coupling of several functional dice together with the respective bond pads of each functional dice operably coupled together through an adjacent die interconnection circuit. Therefore, an adjacent die interconnection circuit that operably couples multiple dice includes a corresponding number of conductor segments that electrically link between a bond pad of one die to the bond pad of the adjacent die, etc. Therefore, by way of example, a semiconductor device comprised of three adjacent functional die would include an adjacent die interconnection circuit that is comprised of a first conductor segment for linking the first and second dice together and then a second conductor segment for linking the second and third dice together.

[0031] The adjacent die interconnection circuit 50 may be fabricated using photolithographic patterning of a deposited metal layer through the use of a single reticle for each type of functional die group (*e.g.*, two dice, three dice, four dice, etc.) which, in the present embodiment may be aligned with each functional die group for the formation of the adjacent die interconnection circuit 50. Such a reticle pattern may accommodate the formation of conductor segments and, additionally, may facilitate the formation of bumped contacts on one or more of the adjacent functional die to form an interconnection pattern as illustrated in FIG. 2. The interconnection pattern illustrated in FIG. 2 couples together functional dice that have an adjacently functional counterpart for the formation of a functional die group.

[0032] FIG. 3 illustrates an alternative embodiment for the coupling of functional dice. In similar manner with the previous embodiment, the individual dice on wafer 60 undergo probe testing for the identification of functional and nonfunctional dice. The test results of the probe testing process are obtained and analyzed to identify adjacent functional dice for the formation of functional die groups. The identification of functional die groups, such as functional die groups 62-70, identifies functional dice candidates for forming into semiconductor devices, namely interconnected functional die groups. In the present embodiment, however, rather than coupling

together only those functional dice which are aggregated into a functional die group, some nonfunctional die are also included within the formation of adjacent die interconnection circuits.

[0033] FIG. 3A illustrates the coupling of functional dice 72-78 through the formation of adjacent die interconnection segments 82-84 for the coupling of their respective bond pads. Similarly, functional die groups 64 and 70 are also routed to adjacent functional die for the formation of the respective semiconductor devices, namely interconnected functional die groups. However, the present embodiment also contemplates formation of the adjacent die interconnection circuits between adjacent functional die by coupling at least some nonfunctional die together with adjacent functional die before segmentation. Such a process may be performed on a portion of the wafer or adjacent die interconnection circuits may be formed throughout an entire die with the coupling of functional die to nonfunctional die being severed during the segmentation process wherein functional and nonfunctional die are diced or segmented.

[0034] Referring to FIG. 4, a memory module in accordance with the present invention, is illustrated as having an elongate carrier substrate 92, such as a printed circuit board (PCB) or other substrate known in the art to which a plurality of functional die are attached. The plurality of functional dice are integral in form and are not individually segmented as in the case of prior art applications but comprise a single contiguous semiconductor substrate and are interconnected with one another according to the formation of the adjacent die interconnection circuits previously described. Coupling of the semiconductor device, illustrated as interconnected functional die group 94, with substrate 92, in one embodiment, may be accomplished through the use of flip-chip bonding wherein the plurality of functional chips are provided with conductive bumps, shown as conductive bumps 42 in FIG. 4A, with each conductive bump 42 electrically coupled to a functionally-like bond pad of each functional die within the interconnected functional die group 94. Interconnected functional die group 94 is operably coupled with substrate 92 by superimposing the conductive bumps 42 over similarly configured substrate contacts or terminal pads 96 on the surface of substrate 92, at which time the conductive bumps 42 (if solder) are heated and melted or "reflowed" to form mechanical and electrical connections between the substrate 92 and functional die group 94. Alternatively, the functional die group 94 may be wire bonded by wire bonds 102 to the substrate 92, as illustrated in FIG. 4B, by wire bonding from adjacent die interconnection segments (*e.g.*, segments 34-38 (FIG. 2A) and segments 82-84 (FIG. 3A)) to substrate contacts 96

which further couple via conductors 98 to PCB electrical contacts 100. The use of TAB connections comprising conductive traces on flexible dielectrics, as well as the use of edge connects in a vertical surface mount configuration, are also contemplated.

[0035] In accordance with a further embodiment, the die group 94 of FIG. 4 may be interconnected one with another, either partially or in totality through conduits 98 on substrate 92. In the present embodiment, the conduits 98 may provide electrical coupling between each of the, for example, conductive bumps 42 (FIG. 4A) rather than rely upon conductive traces formed on the die group 94.

[0036] FIGs. 5 and 5A illustrate another embodiment for coupling together relatively adjacent groups of functional die. In FIG. 5, a wafer 104 is illustrated as having two relatively adjacently located functional die groups 106 and 108 which are separated by a nonfunctional die 110. The present invention contemplates the coupling of relatively adjacent functional die groups, such as functional die groups 106 and 108 into a single semiconductor device, illustrated as interconnected functional die group 112.

[0037] FIG. 5A illustrates the coupling of functional die groups 106 and 108 via bridging nonfunctional die 110 through the use of an adjacent die interconnection circuit 50 described previously. In the present embodiment, the adjacent die interconnection segments 114 couple the functional die of functional die group 106 and adjacent die interconnection segments 116 couple the functional die within functional die group 108. Additionally, the present embodiment further utilizes adjacent die interconnect segments 118 and 120 for bridging an electrical interconnect across the nonfunctional die 110. Following the coupling together of functional die groups 106 and 108, the entire five-die assembly may then be unitarily segmented from the wafer as a semiconductor device, illustrated as interconnected functional die group 112.

[0038] FIGs. 6 and 7 contemplate the deleterious effects associated with having a nonfunctional die within a larger assembly, namely the undesirable aberrational behavior or at least the undesirable additional capacitance associated with unnecessary circuitry attached to adjacent die interconnect segments. In FIG. 6, adjacent die interconnect segments 118 and 120 bridge the coupling of functional die groups 106 and 108 through the coupling of the respective bond pads 122 and 124. However, bond pad 126 of nonfunctional die 110 is isolated through the process of open circuiting a nonfunctional die bond pad isolation conductive segment 128 through a manufacturing

process such as laser ablation or through the use of an etching process through foregoing on interconnection processing step that generates an interconnect between bond pad 126 and conductive segment 128. Alternatively, FIG. 7 depicts the isolation of bond pad 126 from adjacent die interconnect segments 118 and 120 through the use of a gating or isolation device 130 which may be further controlled by an isolation control signal 132. Other forms of isolating bond pad 126 and the associated capacitance and deleterious effects associated therewith are also contemplated as within the scope of the present invention.

[0039] It is also contemplated that various other modules, including memory modules such as a memory module 134 illustrated in FIG. 8 which includes a semiconductor device, namely interconnected functional die group 136, may be incorporated into an electronic system 138, such as a computer system, that includes an input device 140 and an output device 142 coupled to a processor device 144. Of course, the interconnected functional die group 136 may also be incorporated into the input device 140, the output device 142, or the processor device 144.

[0040] The present interconnection approach addresses concerns for accurately routing interconnections to avoid or at least characterize and minimize signal crosstalk. Additionally, module sizes may be minimized by interconnection of various like signals at a device level rather than at a module level. Furthermore, interconnecting bussed signals such as ADDR, RAS, CAS, WE, CLK, CKE greatly reduces interconnections, impedances and their susceptibility to crosstalk and other interference. Signals such as VCC, GND, CS and the DQs preferably are not connected in parallel. The grouped and interconnected parts may then be sawed from the wafer as an individual unit and applied in a system where space sensitivity and routing complexity are appreciated.

[0041] It will be appreciated by those skilled in the art that various circuits and methods can be used to achieve the desired memory capability of the memory module, through the incorporation of a varying number of functional dice which may be coupled to one another through the adjacent die interconnection circuit described herein, or may alternatively be coupled to other functional dice via adjacent nonfunctional die or dice. Those of ordinary skill in the art also appreciated that the number and configuration of the dice, as well as the geometric relationship with other neighboring devices, whether functional or nonfunctional, are also contemplated and the immediate adjacent nature of the functional and nonfunctional die as illustrated herein are but one

example of relationships of a die with other dice on an integral wafer. Additionally, the bonding techniques for attaching and electrically interconnecting the semiconductor device (e.g., interconnected functional die group) with the substrate according to the methods described herein, are also but an example that is not to be considered limiting.

[0042] It will also be appreciated by one of ordinary skill in the art that one or more features of any of the illustrated embodiments may be combined with one or more features from another to form yet another combination within the scope of the invention as described and claimed herein. Thus, while certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the invention disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.